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# **System Level Integration**

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## **V30xx 16 bit CISC CPU Cores**

# Overview

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- **Family Overview**
- **V30HL**
- **V30MX**
- **V30MT**
- **V30MZ**
- **Appendix:**
  - V20 CISC CPU Core
  - Z80 CISC CPU Core

# V30xx - 80186 compatible CISC Controller Overview

Core	CB-C7	CB-C8x	CB-C9x	CB-C10x	Comment
V30HL	20MHz	-	-	-	Compatible with $\mu$ PD70116
V30MX	25MHz	33MHz 1mA/MHz	33MHz	(Note 1)	Enhanced V30ML product
V30MT		20MHz 0.6mA/MHz (note 2)	(Note 1)	(Note 1)	Low-power Version
V30MZ	-	-	66MHz 1.4mA/MHz 35MIPS	(Note 1)	High performance version (0.53MIPS/MHz)

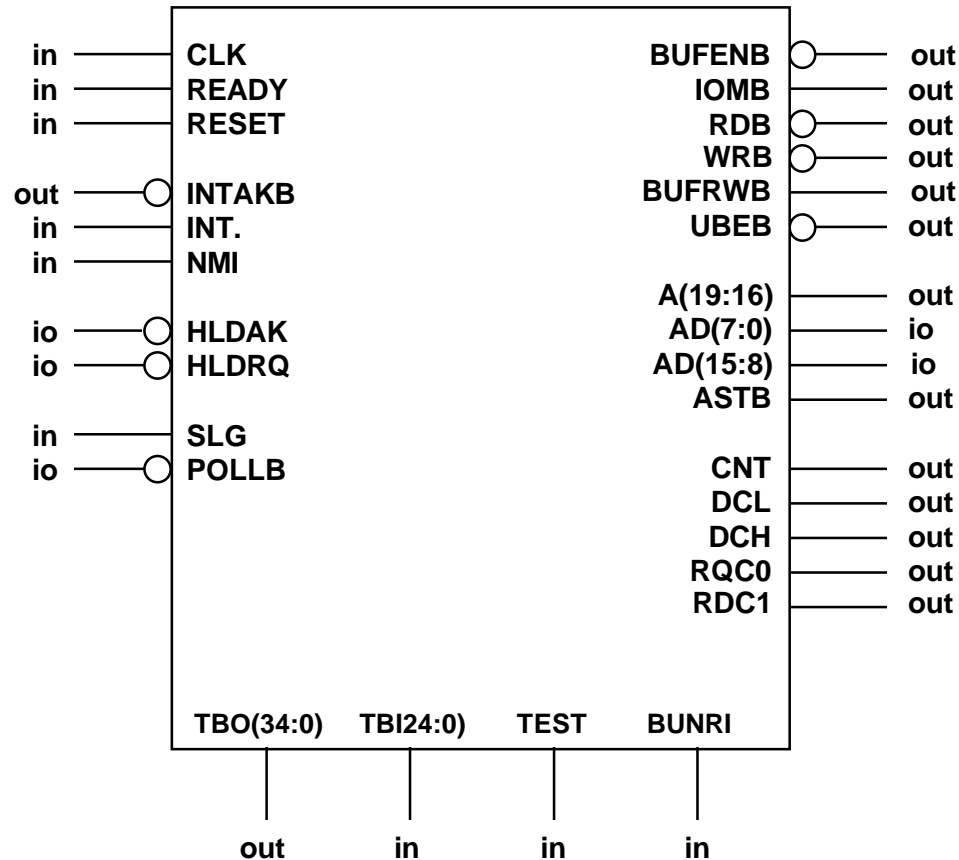
*Note 1: on request*

*Note 2: available on request; Database completed*

# Features of V30HL

- Fully static circuit configuration, the standby mode and clock-stop mode can be easily initiated
- Low power consumption
- Memory addressing size: 1M bytes
- Fourteen 16-bit registers
- 101 different instructions (fully compatible with  $\mu$ PD70116 standard part)
- Widely available emulators and development software
- Example: CB-C7 Implementation
  - 0.8  $\mu$ m CMOS process
  - 20 MHz operation - 2.6MIPS
  - 0,13 MIPS/MHz

# NA70116H 16-Bit CPU Macro (CB-C7)



# Features of V30MX

- Software code compatible with xx286 CPUs
- Fully compatible with V30HL macro and  $\mu$ PD70116H
- 1.67X performance increase over V30HL at same frequency
- 2.8X performance increase at 33 MHz over V30HL at 20 MHz
- LIM EMS 4.0 Register support
- 286 compatible address pipelining allows low cost memory interface
- Example: CB-C8VX/VM Implementation
  - Power consumption 1 mA/MHz
  - 33 MHz operation at 3V - 4.3MIPS
  - 0.13 MIPS/MHz
  - 2.42 x 3.12mm<sup>2</sup>

# Major Differences V30HL vs. V30MX

## ■ Address/Data bus

### ➤ V30HL:

- Address and data bus are multiplexed sharing the same pins
- 24 bit address bus

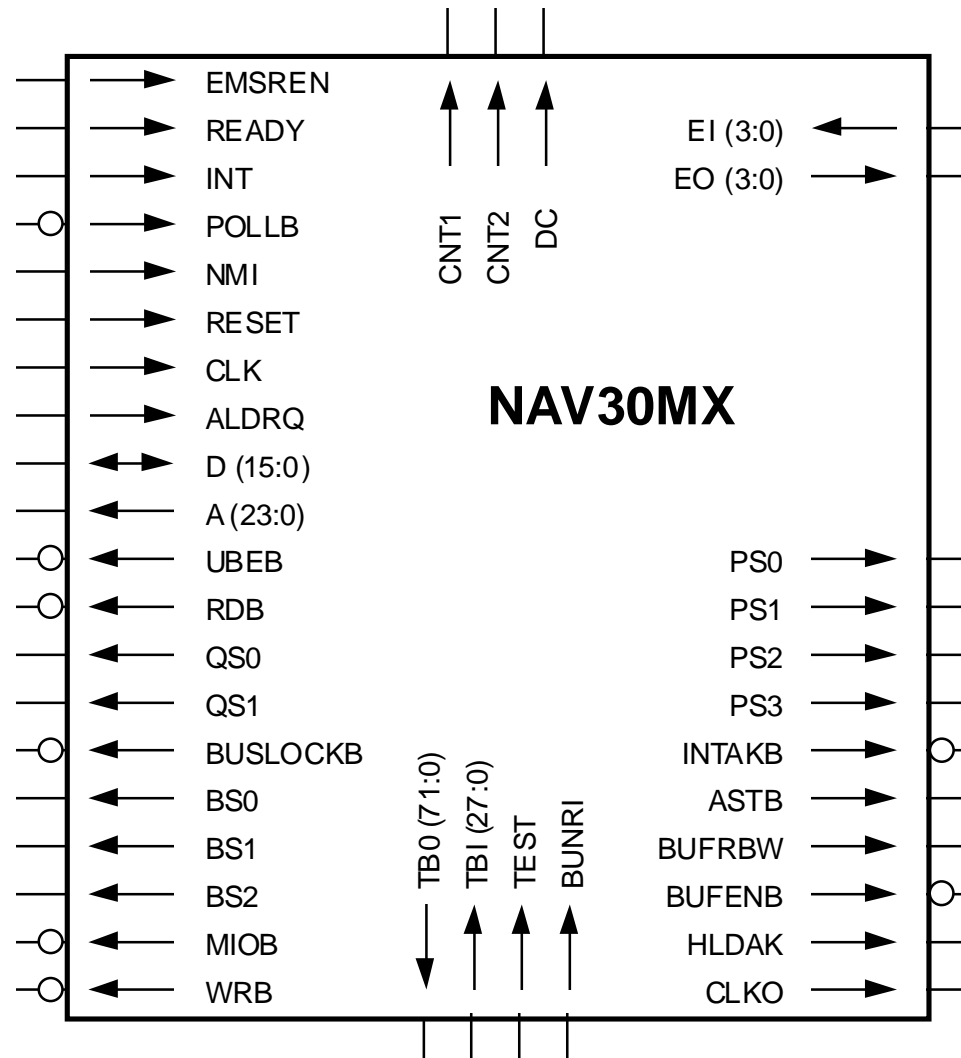
### ➤ V30MX:

- separate pins for address and data bus
- extended address bus (24 bit)

## ■ $\mu$ PD8080AF Emulation Function

- V30HL: support for  $\mu$ PD8080AF Emulation
- V30MX : no support for  $\mu$ PD8080AF Emulation

# V30MX 16-Bit CPU Macro (CB-C8VX)



# Features of V30MT

- **Functionally equivalent to V30MX**
- **Advantages:**
  - Reduced power consumption
  - Reduced area
- **Disadvantage: Reduced maximum computing performance**
- **Example: CB-C8VX/VM Implementation (target data)**
  - 20 MHz operation - 2.6MIPS
  - 0.6 mA/MHz
  - 0.13 MIPS/MHz
  - 2.08mm x 2.08mm

# Features of V30MZ

- **High performance 16bit CISC controller**
- **Completely new design based on internal RISC machine**
- **Fully static circuit configuration, the standby mode and clock-stop mode can be easily initiated**
- **Memory addressing size: 1M bytes**
- **0.53 MIPS/MHz instead of 0.13 MIPS/MHz for V30MT/MX**
- **Instruction set is the same one as 80186 of Intel Inc.**
  - Support for expanded instruction set of V30HL/MX/MT, EMS 4.0 and 8080 emulation mode have been skipped to optimize cost efficiency
- **Widely available emulators and development software**
- **Example: CB-C9 Implementation**
  - 66 MHz operation - 35 MIPS
  - 1.4mA/MHz power consumption
  - 2.3mm x 2.3mm

# Appendix: V20

- **For NEC's 0.8 and 0.5 micron CB-IC families (CB-C7 and CB-C8VX/VM) also the Intel 8086 compliant V20 CPU core is available**
  - 16 bit microprocessor
  - 8 bit databus
- **CB-C7 implementation**
  - Size: 3.7 x 3.9 mm<sup>2</sup>
  - Clock: 8 MHz
  - Performance: 0.4 MIPS
- **CB-C8 implementation**
  - Size: 1.7 x 1.7 mm<sup>2</sup>
  - Clock: 20 MHz
  - Performance: 1 MIPS

# Appendix: Z80

- For general low-end controller application or for flexible software implementations of fixed functions NEC offers Zilog Z80 compatible CISC CPU cores in all cell-based technologies
- **CB-C8VX/VM**
  - Size: 1.7 x 1.7 mm<sup>2</sup>
  - Clock: 20 MHz
- **CB-C9**
  - Size: 1.1 x 1.1 mm<sup>2</sup>
  - Clock: 33 MHz